PDB Design in the Next Generation 800 VDC Architecture

I. Introduction

Currently, with the explosive growth of computing power demands such as AI large - model training and the expansion of cloud computing service scales, data centers are experiencing an unprecedented wave of power density leap. The power of a single cabinet has rapidly evolved from the traditional kW - scale racks and is about to enter the new stage of MW - scale power racks in the future. This imposes significant challenges to the carrying capacity, efficiency, and stability of the power supply system.

The traditional data center power architecture relies on 54 VDC bus and uses bulky copper bus-bars to transmit electricity from power rack to server trays. This model has gradually reached physical limits when rack power exceeds 200 kilowatts. Firstly, at the MW scale, power shelves occupy substantial rack space, leaving little to no room for computing equipment. Secondly, the physical constraints of using 54 VDC in a single 1 MW rack require up to 200 kilograms of copper bus-bars. Scaling to a 1 GW data center, the rack-mounted bus-bars alone could require up to 500,000 tons of copper. Clearly, the current power distribution technology is unsustainable for the future of GW-scale data centers.

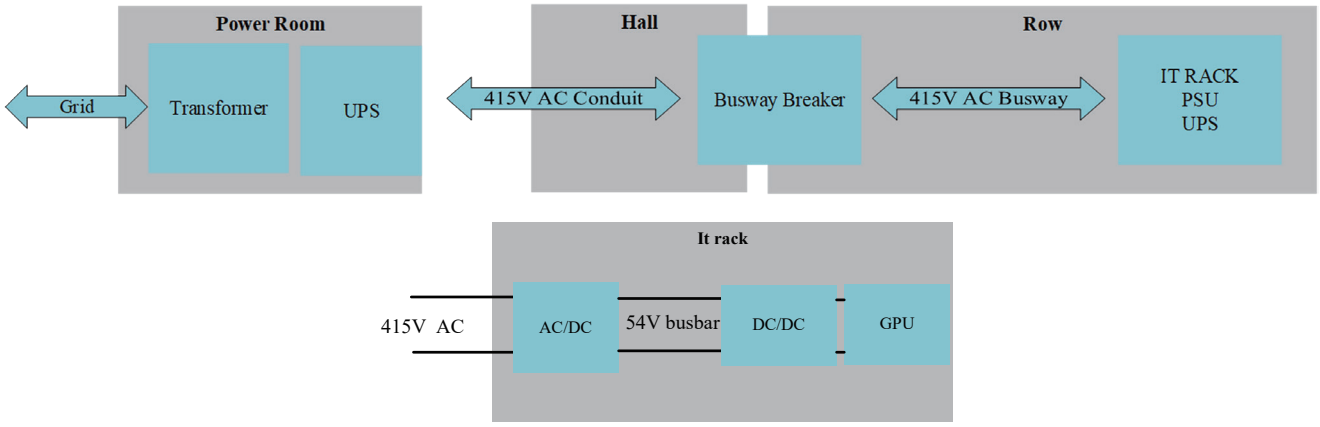
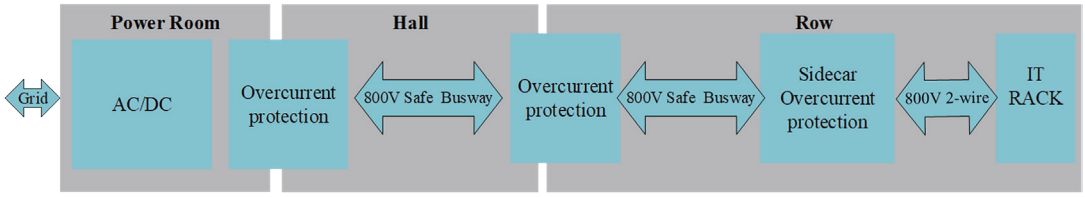


Fig. 1 Traditional Data Center 54VDC Power Architecture

The 800 VDC solution uses industrial-grade rectifiers to directly convert 13.8 kV AC grid power to 800 VDC, eliminating most intermediate conversion steps. This simplifies the power architecture, reduces electrical system complexity, and enhances the overall reliability of the system. At the same time, it also significantly reduces losses from repeated AC/DC, DC/DC conversions and power transmission—making it a more effective power distribution solution for modern data centers. 800 VDC architecture is shown in the Figure 2.



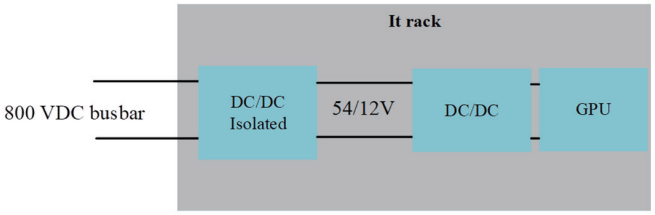


Fig. 2 800 VDC Power Architecture

In the 800 VDC architecture, the Power Distribution Board (PDB) acts as a critical hub linking the high-voltage DC main bus to downstream IT equipment. Its core function is to distribute centrally input high-voltage DC power into multiple channels of current or voltage tailored to load requirements. By integrating features like hot-swapping, overvoltage/under voltage/overcurrent protection, and PMBus (Power Management Bus) status monitoring, the PDB provides end devices with a safe and reliable power supply.

Critically, the hot-swap capability delivers unique value: it enables data centers to safely insert, remove, or replace the PDB while the system remains energized, without disrupting power supply to other devices. This capability not only mitigates the risk of computing power interruptions during equipment maintenance but also significantly shortens fault recovery times. For scenarios such as AI data centers—where 24/7 continuous operation is essential—this function directly enhances the availability and operational efficiency of the power supply system. In large-scale data centers, according to industry statistics, the loss caused by each hour of downtime can reach tens of thousands of dollars or even more. Take a medium-sized data center as an example. Assuming that its hourly downtime loss is about 50,000 dollars, when traditional PDBs break down, replacement requires a downtime of about 2 hours, and the direct loss caused by each failure is about 100,000 dollars. When a failure occurs, PDBs integrated with functions such as hot-swap show great advantages. Firstly, they can quickly respond to failures and cut off abnormal circuits, preventing the spread of failures and ensuring the stable operation of equipment. Secondly, hot-swap PDBs do not require downtime for replacement, which can compress the fault recovery time to 10-15 minutes. The Mean Time to Repair (MTTR) is shortened by more than 90%, which can basically avoid downtime losses.

Subsequent sections will further explore the technical principles of the PDB in 800 VDC architectures, the implementation mechanism of its hot-swapping function, and its quantifiable impact on operational efficiency and system reliability in practical scenarios—providing insights for data centers considering power architecture upgrades.

II. Technical Implementation of PDB

2.1 Function Block of PDB

As shown in Figure 3, a PDB integrates many key functional components, including a high-voltage input unit, an auxiliary power supply unit, and hot-swap unit. The high-power-density DC/DC power unit, standby power supply unit, Signal control and PMBus communication unit, input capacitor (Cin), output capacitor (Co), output connection connector, and so on.

The high-voltage input unit includes high-voltage input connector, TVS (Transient Voltage Suppressor), and fuses. It can effectively prevent damage to downstream components caused by overvoltage/overcurrent, thus ensuring the safety and reliability of the high-voltage circuit. The auxiliary power supply unit provides appropriate power supply voltages (such as 12 V or 5 V) for circuits inside the PDB, including hot-swap control circuits and communication monitoring circuits. The hot-swap unit, comprising a hot-swap controller and an electronic fuse (eFuse), primarily functions to prevent large inrush currents and mitigate electrical disturbances during board insertion and removal operations. The high-power-density DC/DC power transmission unit steps down the 800V direct current to voltages

suitable for loads (such as 50 V or 12 V) and enables high-power transmission. The signal control and PMBus communication unit is used to control and regulate the hot-swap and DC/DC power units, as well as monitor parameters such as voltage, current, and temperature inside the PDB.

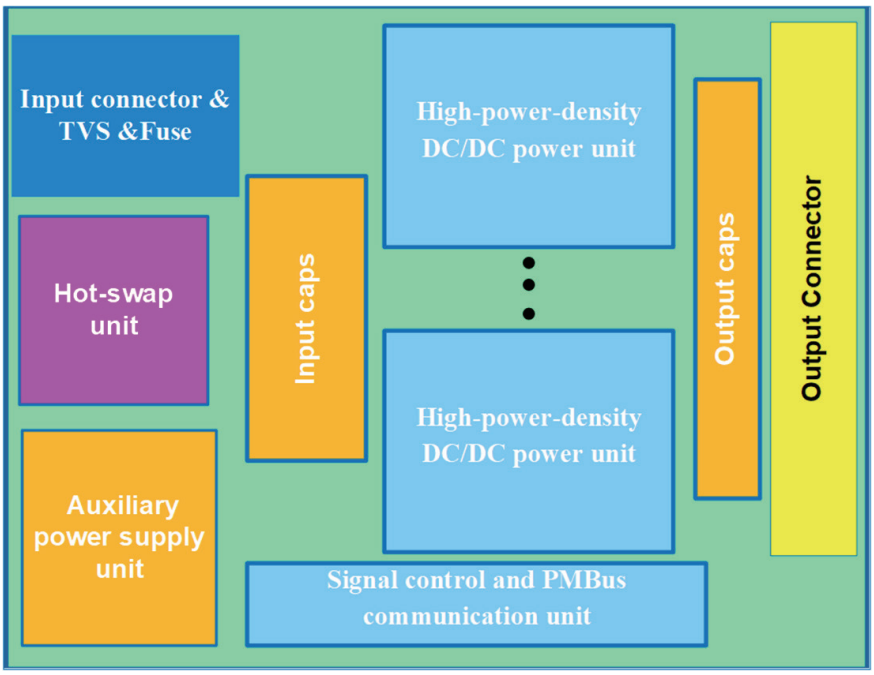


Fig. 3 The functional block diagram of PDB

2.2 Implementation of Hot-Swap Technology

2.2.1 Fundamental Principles of Hot-Swap Operation

Each PDB that is hot-swapped into an 800 VDC system includes capacitors as the first energy storage and filtering out voltage ripple and high-frequency noise. The capacitor at the time of the insertion acts as a short or low-impedance path from the 800V input voltage to the ground. If at this moment, the PDB is hot-swapped into the 800 VDC, a significant inrush current will be generated in a short period—strong enough to blow the fuse or cause a noticeable voltage drop. This could trigger a system-wide shut down for adjacent connected server trays. By increasing the resistance of the current path, i.e. the impedance between the 800 VDC and Cin, the inrush current can be limited to a desired value.

The hot-swap unit integrated into the PDB can effectively achieve this purpose. When the PDB is inserted into the 800 VDC system, the auxiliary power supply unit is first connected to supply power to the hot-swap controller, allowing the controller to start up first. Subsequently, the hot-swap controller adjusts the gate voltage (Vgs) of the MOSFET to make it operate in the linear/saturation region. At this point, the path impedance from the 800 VDC to Cin is dominated by the high Rds (on) of the MOSFET, and the charging current of Cin is limited to a low level, thus avoiding initial inrush current, as shown in Figure 4. Meanwhile, the hot-swap controller monitors the voltage of Cin and the current through the MOSFET (Iin) in real time. As the Cin charges slowly, the controller synchronously and gradually increases the Vgs of the MOSFET, causing its Rds (on) to decrease gradually, ensuring that the charging current remains stable at the set limit value. Finally, when the voltage of Cin approaches 800V, the controller fully turns on the MOSFET (Rds (on) drops to the minimum, usually a few milliohms), and the impedance of the main power path returns to normal. Eventually, the PDB completes hot insertion and then supplies power to the load according to normal logic, and the inrush current suppression process ends.

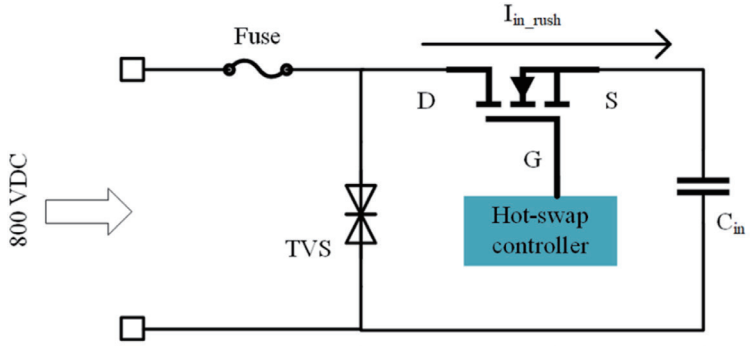


Fig. 4 inrush current control during insertion

During the PDB extraction process, the key is to avoid arc generation, which would ablate the interface. This is achieved by means of the timing control and rapid turn-off function of the hot-swap unit. When it is detected that the PDB starts to detach from the interface, the hot-swap controller quickly turns off the MOSFET to block the discharge path from Cin to the system. After the main power path is completely disconnected, the interface is physically detached, and no current flows at this time, thus avoiding arc generation and preventing system voltage fluctuations caused by PDB detachment.

2.2.2 Key Components Enabling Hot-Swap Functionality

The hot-swap functionality in PDBs is enabled by a synergy of specialized components, each playing a critical role in ensuring safe and stable insertion and removal of modules. At the core of this system are dedicated hot-swap controller ICs, such as specific models from leading manufacturers, which act as the "brain" managing the entire insertion and removal process. These controllers bring a host of advanced features: precise current sensing allows them to monitor current flows with high accuracy, programmable current limits let engineers set safe thresholds tailored to the system's needs, and integrated over-temperature protection shuts down operations if temperatures rise beyond safe levels to prevent component damage. Additionally, fault reporting capabilities provide real-time feedback on issues like overcurrent or overvoltage, facilitating quick diagnostics and maintenance. Furthermore, it is of great significance that these controllers are responsible for ensuring that MOSFETs are not damaged during hot swapping and remain within their design limits. The design limits are defined by the Safe Operating Area (SOA) curve in the MOSFET data sheet. As an example, the SOA curve of SUPERFET V MOSFET NTHL017N60S5H of ONSEMI is shown below:

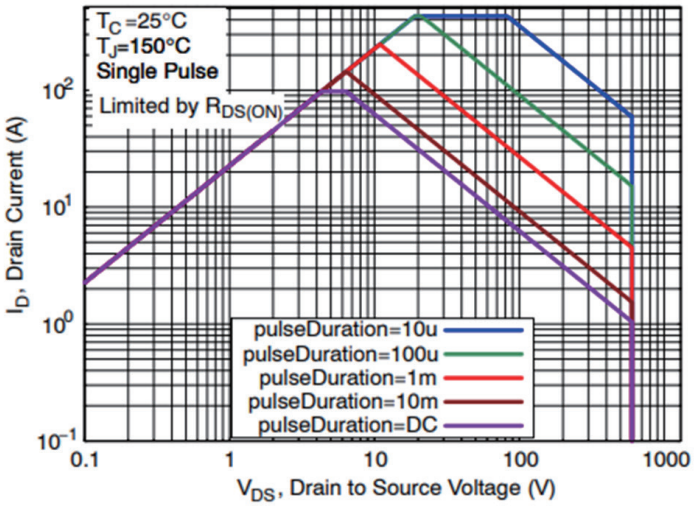


Fig. 5 SOA curve of NTHL017N60S5H

The SOA curves show the amount of drain current the MOSFET can handle with the applied VDS across it. From the SOA curve, we can see that as VDS decreases, the drain current allowed to pass through the MOSFET increases. Also, the current handling capability of the FET increases further if the duration of the current pulse across the MOSFET is reduced. As shown in Figure 5, when the FET is operated on the 1ms SOA line，the current handling capability increases compared to when it is operated on the 10ms or DC SOA line. For hot-swapping applications, it is generally considered to be safe to design for operation at the DC SOA line.

Complementing the controllers are MOSFETs and various passive components, which form the "muscle" of the hot-swap circuit. The selection of MOSFETs is critical, with criteria including voltage rating that matches the PDB's high-voltage input, low on-resistance to minimize power loss during operation, and robust SOA characteristics to withstand transient conditions during hot swapping. Current-sense resistors or integrated current sensors are essential for providing real-time current feedback to the hot-swap controller; by detecting current levels, they enable the controller to adjust operations dynamically, such as triggering current limiting when thresholds are exceeded. Capacitors also play a vital role as energy storage devices, smoothing out voltage fluctuations and stabilizing the supply during the sudden current demands of insertion, while resistors are used for current limiting in specific paths and for discharging capacitors safely when PDBs are removed, preventing residual voltage hazards.

Mechanical and connector design is equally fundamental to reliable hot-swap functionality. Hot-swap connectors must meet stringent requirements: they feature robust construction to withstand repeated use, reliable mating to ensure consistent electrical contact, and appropriate contact sequencing. For insertion, long pins (typically for ground and control signals) make contact first to establish a stable reference and enable pre-insertion checks, while short pins (for power or sensitive signals) connect later once conditions are safe; during removal, the sequence is reversed, with short pins disconnecting first to minimize interference. These connectors also need a high cycle life, often with a minimum of 500 insertion/removal cycles to meet long-term operational needs. Beyond connectors, mechanical interlocks and guides prevent incorrect insertion—interlocks may block mating if a PDB is misaligned, while guides ensure precise alignment during insertion, reducing the risk of damage to pins or components and ensuring the hot-swap process proceeds smoothly.

2.3 Design of High Power Density DC/DC Power Units

In the 800 VDC architecture's PDB, the DC/DC power unit serves as a crucial component for voltage conversion and power transmission. It undertakes the task of stepping down the 800 VDC from the bus to 50 V/12 V, which is suitable for the operation of downstream devices like servers, while stably transmitting the required power to these devices, ensuring their reliable energy supply.

When it comes to the performance of the DC/DC power unit in the PDB, several aspects need key attention. Firstly, conversion efficiency is vital—high efficiency reduces power loss, which aligns with the energy-saving demands of the 800 VDC architecture. Secondly, voltage regulation accuracy is essential; the 50 V output must remain stable within a small deviation range to avoid affecting the normal operation of downstream devices. Additionally, dynamic response performance matters greatly. It should quickly adapt to load changes of downstream devices, minimizing voltage fluctuations during load transitions.

The DC/DC power unit also faces critical design challenges. One major challenge is heat dissipation. Operating under high voltage and power conditions leads to significant heat generation, and effective heat dissipation designs are required to prevent performance degradation or even damage due to overheating. Another challenge is ensuring high reliability. The unit needs to maintain stable operation in complex data center environments for long periods, withstanding factors like voltage fluctuations and temperature variations. Moreover, achieving a compact structure is challenging too, as the PDB has

limited space, and the DC/DC power unit must be designed to be small in size while meeting performance requirements. Therefore, in the design of the ±400 V/800 V DC/DC power unit, the selection of topology is of great importance.

Currently, the available topologies include the two-level half-bridge series LLC topology, the three-level series half-bridge (TL SHB) LLC topology, and the two-level half-bridge topology. Among them, the two-level half-bridge topology is shown in Figure 6. Due to the limitations of the topology itself, it requires the use of switching devices with a withstand voltage of over 1000 V. These switches are relatively large in size, which is not conducive to achieving high power density of the module in the 800 V PDB. Moreover, since the transformer voltage is only 1/2 Vin, the core volume is relatively large. Because of these obvious drawbacks, the two-level half-bridge topology is not discussed in this context.

The two-level series half-bridge LLC topology can avoid the above shortcomings, and its topology structure and switch control timing are shown in Figure 7. This topology can be matched with 650 V gallium nitride (GaN) series power switches, which is highly beneficial for achieving high efficiency and high power density. In addition, by interleaving the control of switch timing, this topology can effectively reduce the ripple current on the output capacitor, thereby reducing the output voltage ripple and AC losses at the output end. This has been fully verified by the comparison of simulation results, as shown in Figure 8.

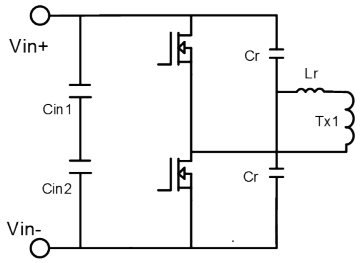


Fig. 6 Two-level half-bridge topology

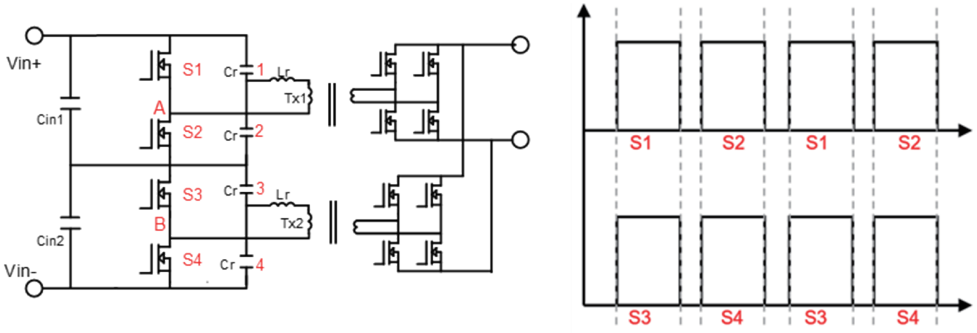


Fig. 7 The two-level half-bridge series LLC topology and switch control

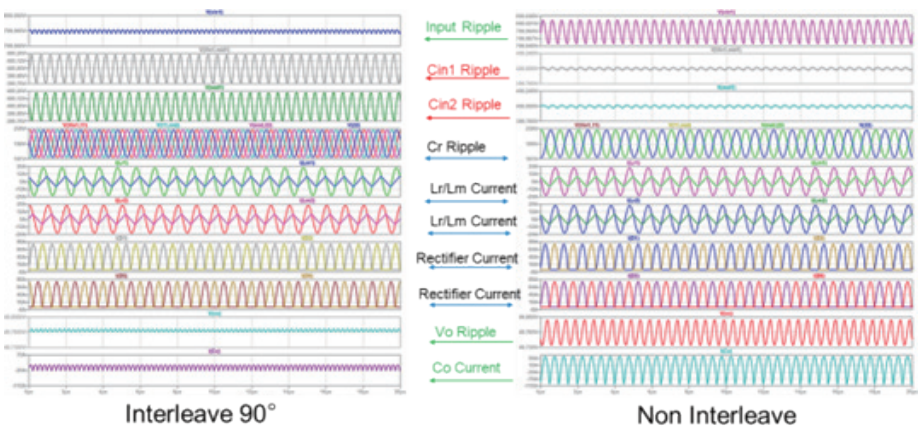


Fig. 8 Simulation waveforms of interleave and without interleave control

Similarly, the Three-Level Semi-Bridge (TL SHB) topology and in-phase control timing are shown in Figure 9. However, due to non-ideal factors such as line capacitance and asymmetric drive pulse width, during actual operation, it often leads to a gradual imbalance in the voltage of the input bus voltage-dividing capacitors. This, in turn, causes an increase in the voltage stress of the power switches, resulting in the loss of the original advantages of the three-level topology. In severe cases, there is even a potential risk of switch damage due to overvoltage. By adjusting the phase of the drive signal in the in-phase control mode, the voltage of the input bus voltage-dividing capacitors can be balanced.

This topology can also operate in the double-frequency mode, and its control timing is shown in Figure 10. In the frequency-doubling mode, even if there is a duty mismatch, although there will be a static error in the voltage of the bus voltage-dividing capacitors, it will not gradually become imbalanced. However, this simultaneously leads to a significant increase in the conduction loss of the primary-side switches: the conduction loss of Q1 (Q4) is twice that of Q1 (Q4) in the two-level semi-bridge series topology, and the conduction loss of Q2 (Q3) is three times that of Q2 (Q3) in the two-level semi-bridge series topology. Under the same conditions, the comparison of the simulated current waveforms of the primary-side switches is shown in Figure 11. This is extremely unfavorable for improving efficiency and optimizing heat dissipation performance. Meanwhile, since there is a large difference between the initial voltage of the flying capacitor and the steady-state capacitor voltage, a pre-charging circuit or other methods are required.

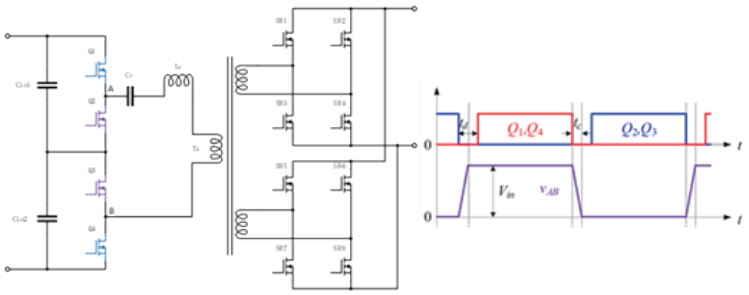


Fig. 9 TL SHB topology and in-phase control timing

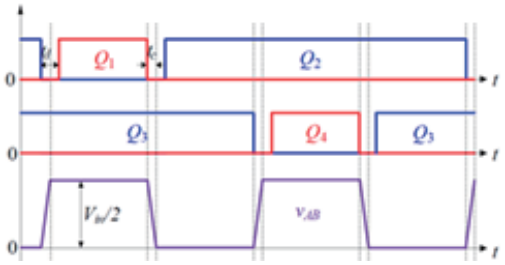


Fig. 10 Control timing in double-frequency mode of TL SHB

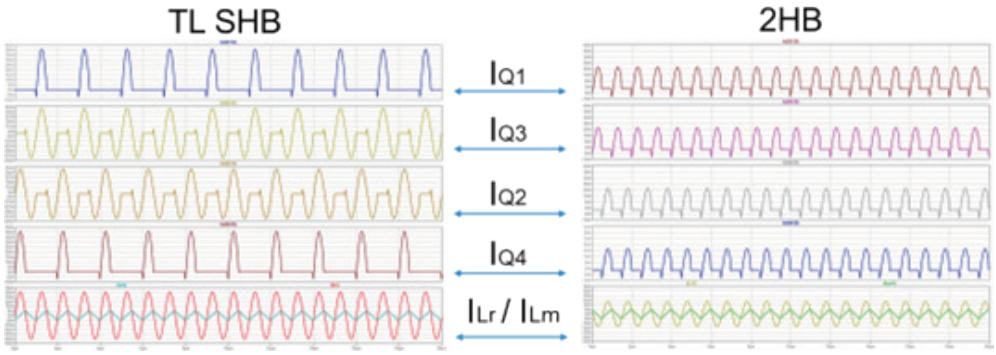


Fig. 11 The primary side switch current waveforms of TL SHB and 2HB

In summary, the two-level series half-bridge LLC topology demonstrates significant advantages in terms of efficiency, power density, dynamics, and reliability in 800V PDB applications.

III. Key Performance Indicators of PDB

To ensure the stable application of PDBs in the 800 VDC architecture across various data center scenarios, it is necessary to conduct multi-dimensional testing and verification work to comprehensively assess their performance, reliability level, and safety compliance. The following elaborates in detail from three aspects: key performance, reliability, and safety regulations.

In the 800 VDC architecture of data centers, the key performance of PDB focuses on conversion efficiency, dynamic performance, hot-swappable performance, and thermal performance. Conversion efficiency is the core measure of PDBs' energy utilization capability, particularly crucial in the 800 VDC architecture as it directly relates to the entire data center's energy consumption. For every 1 % increase in efficiency, significant energy waste can be reduced in large-scale deployments. Testing should cover efficiency under rated (usually required to reach 97 % or higher), light, and overload conditions—low light-load efficiency leads to prolonged "low energy efficiency operation," while poor overload efficiency stability affects the system's ability to handle sudden high loads. The physical object of Delta's 800V PDB is shown in Figure 12. The efficiency data of the power unit in Delta's 800 V hot-swap PDB is shown in the Figure 13.

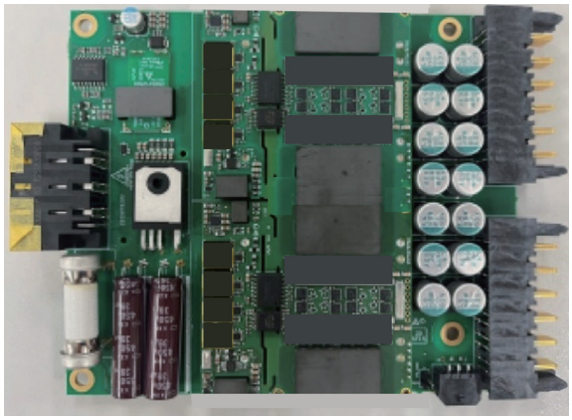


Fig. 12 photo of Delta's 800V PDB

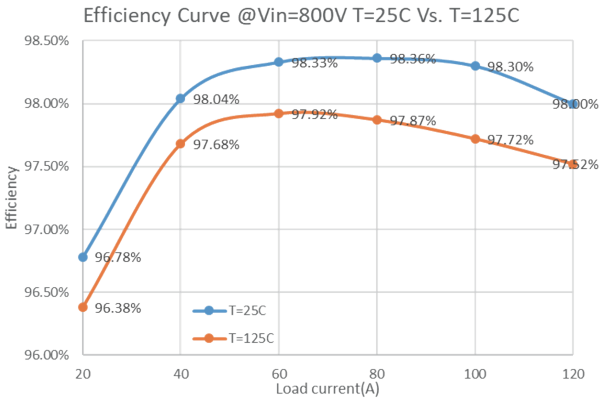


Fig. 13 The efficiency of the power unit in PDB

Dynamic performance determines how quickly PDBs respond to sudden load changes of downstream devices. In data centers, server loads often fluctuate sharply with business needs, such as jumping from 20 % load to 80 % load instantly. PDBs must respond swiftly, with output voltage overshoot controlled within 5 % and recovery time to stability less than 100μs; poor dynamic performance may cause server chip restarts or data transmission issues, affecting business continuity.

The hot-swap function must provide reliable guarantees for three key scenarios: limiting inrush current when the PDB is inserted, avoiding arc generation when it is pulled out, and quickly cutting off the circuit in the event of a fault. Delta's 800 V to 50 V PDB performs excellently in these aspects. It can limit the inrush current to a low level during insertion and quickly cut off the MOSFET when a fault occurs, with relevant characteristics shown in Figures 14 and 15.

Specifically, during the insertion phase, the PDB controls the gate voltage (Vgs) of the MOSFET to make it operate in the linear region, thereby stably limiting the inrush current to approximately 100 mA. After the input capacitor finishes charging, the MOSFET will be fully turned on to ensure the normal operation of the main power path. When a system fault occurs, the hot-swap controller can quickly turn off the MOSFET with a delay at the microsecond level, promptly cutting off the power circuit and effectively preventing the spread of the fault.

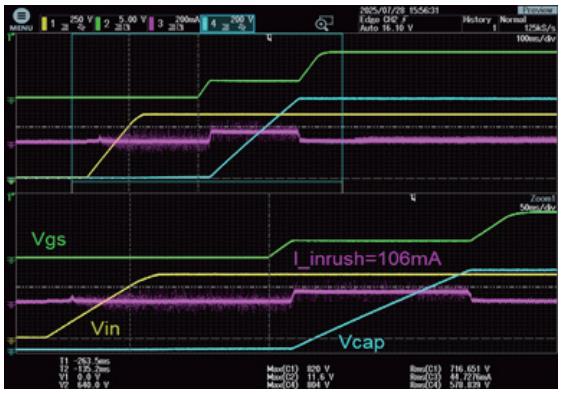


Fig. 14 Inrush current limitation during PDB insertion

Fig. 15 MOSFET fast turn-off response under fault conditions

Thermal performance relates to PDBs' long-term stable operation. Under 800 V high-power conditions, internal components like power switches and transformers generate continuous heat; inadequate heat dissipation may cause core components to exceed safe temperatures. Attention should be paid to temperature rise curves—under full-load operation, the difference between shell temperature and ambient temperature should be less than 70°C—and uniform temperature distribution of key components to avoid local "hot spots." Good thermal performance delays component aging, extends MTBF, and reduces maintenance costs.

Reliability testing verifies long-term stable operation, with plans designed for data centers' complex environments. Environmental adaptability testing includes high-low temperature cycles (such as -40 °C to 70 °C) and humidity alternating tests to check component stability under temperature changes and high humidity, preventing issues like solder joint cracking. Voltage fluctuation impact testing simulates grid voltage changes (such as ±10 % voltage jump) to verify PDBs' anti-interference ability. Durability testing involves long-term load operation (such as continuous full-load operation for over 5000 hours), by monitoring key component parameters to evaluate aging and predict service life. Vibration testing simulates transportation or installation vibrations (e.g., 10-2000 Hz frequency range) to inspect internal structural strength, avoiding component loosening or falling.

Safety compliance testing is essential for meeting industry standards. Insulation performance testing includes measuring insulation resistance (requiring a minimum of 100 MΩ at 500 VDC voltage) and conducting dielectric strength tests (applying a high AC voltage such as 2500 V RMS between isolated circuits for a specified time, usually 1 minute) to prevent electric shock. Overcurrent and overvoltage protection testing verifies PDBs can trigger protection mechanisms promptly when output current exceeds 150 % of the rated value or output voltage exceeds 110 % of the nominal value, avoiding damage. Temperature rise testing ensures surface temperature stays within safe limits (usually 70 °C higher than ambient temperature) during full-load operation. Electromagnetic Compatibility (EMC) testing checks compliance with emission and immunity standards—ensuring PDBs don't generate excessive interference and can operate normally amid external electromagnetic disturbances (such as radio frequency interference or electrostatic discharge).

IV. Summary

Against the backdrop of the dramatic increase in data center power density, the traditional 54 VDC architecture has become unsustainable due to issues such as high space occupancy and large copper busbar demand. The 800 VDC architecture has thus emerged as a better solution, with the PDB serving as a critical hub within this architecture. Technically, the PDB integrates multiple key functional units. Its hot-swap technology enables safe insertion and removal through rational control principles and component synergy, and the two-level series half-bridge LLC topology adopted in its DC/DC power unit offers significant advantages in terms of efficiency and other aspects.

In terms of performance, the PDB excels in key indicators like conversion efficiency and hot-swap performance. Taking Delta's relevant products as an example, they are highly efficient, can effectively respond to faults, and can adapt to complex data center environments after multi-dimensional testing. Overall, this PDB can address the challenges of traditional architectures, deliver significant value in loss reduction and efficiency improvement, and provide support for the stable and efficient operation of modern data centers.

Learn more about Delta's 800 VDC Power Solutions Showcased at OCP Global Summit 2025:
https://www.delta-americas.com/en-US/news/deltas-groundbreaking-800-vdc-power-solutions-showcased-at-ocp-global-summit-2025-to-enable-sustainable-ai-factories