Smart Discrete GaN 700V Power Transistor

FET-E70D040B10

Datasheet Rev. V00

ANCORA

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FET-E70D040B10

Smart Discrete GaN 700V Power Transistor

1. Description

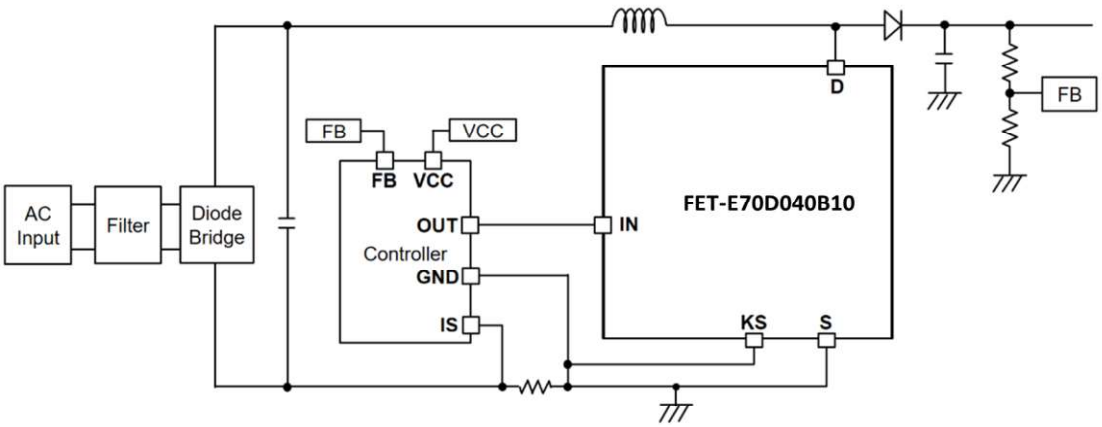
Features

- 700V E-mode GaN FET
- DFN 8x8mm
- Long Time Support Product for Industrial Applications
- Wide Operating Range for IN Pin Voltage
- Low Propagation Delay
- High dv/dt Immunity
- Adjustable Gate Drive Strength
- De-saturation Protection
- Active Miller Clamp
- Thermal Shutdown Protection
- IN Voltage Range: 8.5 V to +20 V
- Allowable Input Switching Frequency: 2 MHz (Max)
- GaN HEMT D-S ON State Resistance: 40 mΩ (Typ)

Applications

Industrial Equipment, Power Supplies with High Power Density, High Efficiency Demand, or Bridge Topology such as Totem-pole PFC, LLC Power Supply, Adaptor, etc

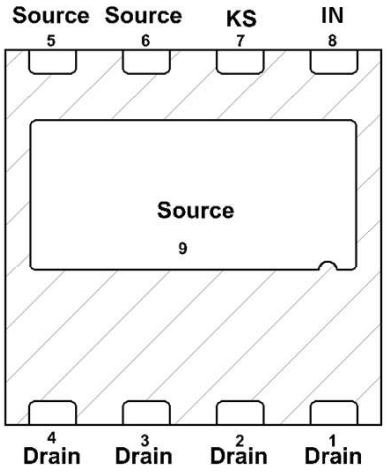
Typical Application Circuit



Pin Configuration

TOP View

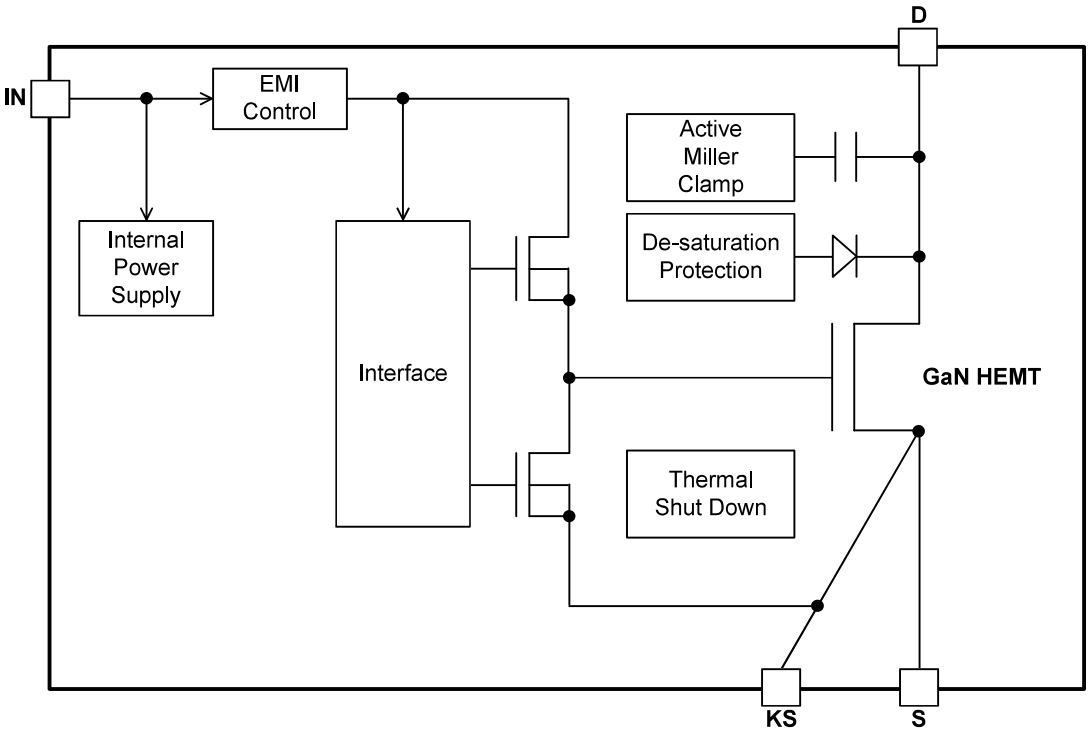
Bottom View



Pin Decriptions:

Pin Number	Pin Name	I/O	Function
5-6, 9	S	O	GaN HEMT Source pin
7	KS	O	GaN HEMT Kelvin Source pin
8	IN	I	Non-inverting gate drive input pin
1-4	D	I	GaN HEMT Drain pin

Block Diagram:



2. Overview

The IC, which integrates GaN device and other additional functions such as protections, offers an optimum solution for making high power density design much easier and more efficient.

Due to a zero reverse recovery and extremely low output capacitance of GaN device, the IC achieves excellent efficiency especially in bridge-based topologies. It is also possible to replace existing Si MOSFETs and heatsinks to improve the efficiency and PCB size.

The integrated circuit with wide operating the IN pin input voltage range brings a remarkable switching performance such as a high drain slew rate and low propagation delay, and it also makes the GaN device even much easier to use than traditional Si MOFET discrete.

Furthermore, various protections also contribute to reliability and robustness and protects this IC from damages.

3. Feature Descriptions

3.1 GaN HEMT

This IC integrates an enhancement-mode (normally-off) GaN device.The enhancement-mode GaN device has smaller parasitic inductance and less switching loss than the cascode topology which connects a depletion-mode (normally-on) GaN device and a Si MOSFET in series because the cascode topology has additional parasitic inductance between a depletion-mode GaN device and Si MOSFET. These characteristics offer advanced switching performance physically, and that is significant especially in large current applications.

3.2 EMI Control

Generally, there is a tradeoff between efficiency and EMI. A higher switching slew rate reduces the switching loss, in the other hand, it also increases the switching noise. By resistance between the IN pin and an external driver IC's output pin, the turn-on slew rate SR_{ON} and the turn-off slew rate SROFF can be adjusted. It is recommended that an external driver IC's output source or sink current capability is more than 500 mA. It allows users to optimize the switching speed according to specific circumstance, such as an EMI filter space, PCB layout, etc.

Turn-on and turn-off sequence is shown in Figure 1.

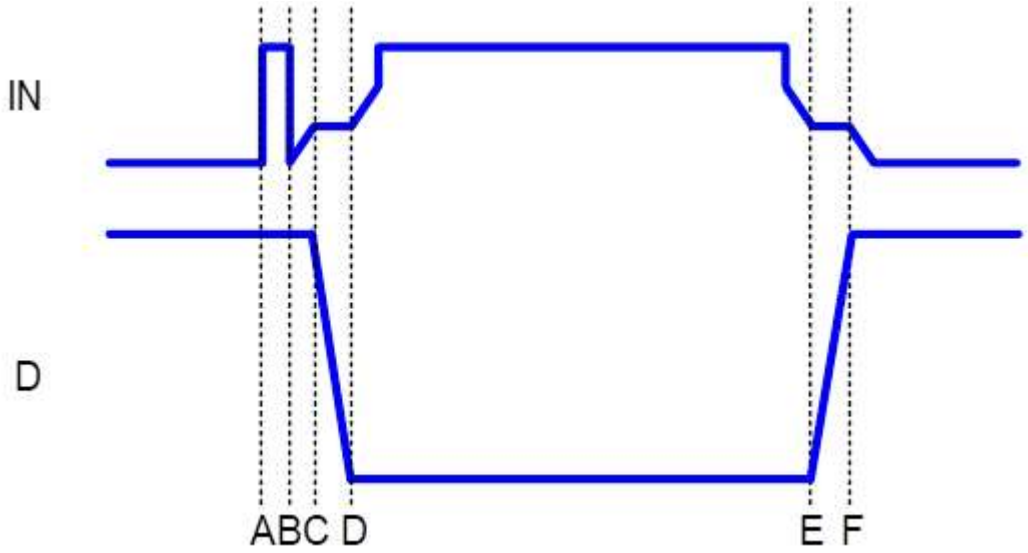


Figure 1. Turn-on and Turn-off Sequence Timing Chart

A: The IN pin voltage goes high.
B: After IC's logic propagation delay from A, gate voltage of GaN HEMT starts to rise. The glitch appear in the IN pin voltage because the charge suddenly moves to gate capacitance of GaN HEMT. To prevent malfunction, the IC masks the glitch.
C: Gate voltage of GaN HEMT reaches the plateau, and the D pin voltage starts to fall.
D: The D pin voltage finishes to fall. The slew rate from C to D is controlled by R_{INON}.
E: Gate voltage of GaN HEMT reaches the plateau, and the D pin voltage starts to rise.
F: The D pin voltage finishes to rise. The slew rate from E to F is controlled by R_{INOFF}.

3.3 Active Miller Clamp

When dv/dt higher than dv/dt_{AMC} occurs at the D pin, the active miller clamp function operates and the gate of GaN HEMT is pulled down. The self-turn-on of GaN HEMT is prevented due to this function.This function does not affect SR_{OFF} because this function is activated only when GaN HEMT's gate is less than plateau voltage.

3.4 De-saturation Protection

De-saturation protection sequence is shown in Figure 2.

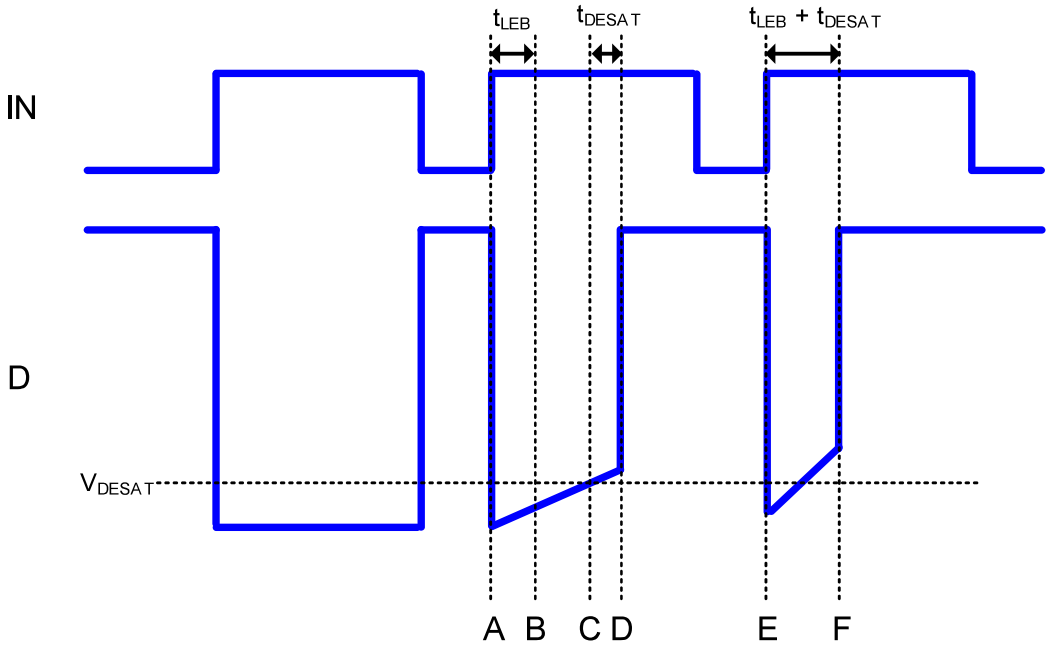


Figure 2. De-saturation Protection Sequence Timing Chart

A: The IN pin voltage goes high and GaN HEMT turns on, and D pin voltage falls.
B: During t_{LEB} from A to B, de-saturation protection is masked.
C: GaN HEMT starts to be saturated and D pin voltage exceeds V_{DESAT}.
D: After t_{DESAT} from C, GaN HEMT turns off by de-saturation protection.
E: GaN HEMT can turn on again because de-saturation protection is pulse by pulse protection.
F: When D pin voltage exceeds V_{DESAT} during t_{LEB} from E to F, GaN HEMT turns off after t_{LEB} + t_{DESAT} from E by de-saturation protection.

3.5 Thermal Shut Down

This IC has thermal shut down function.

4. Starup Sequence

Startup sequence is shown in Figure 3.

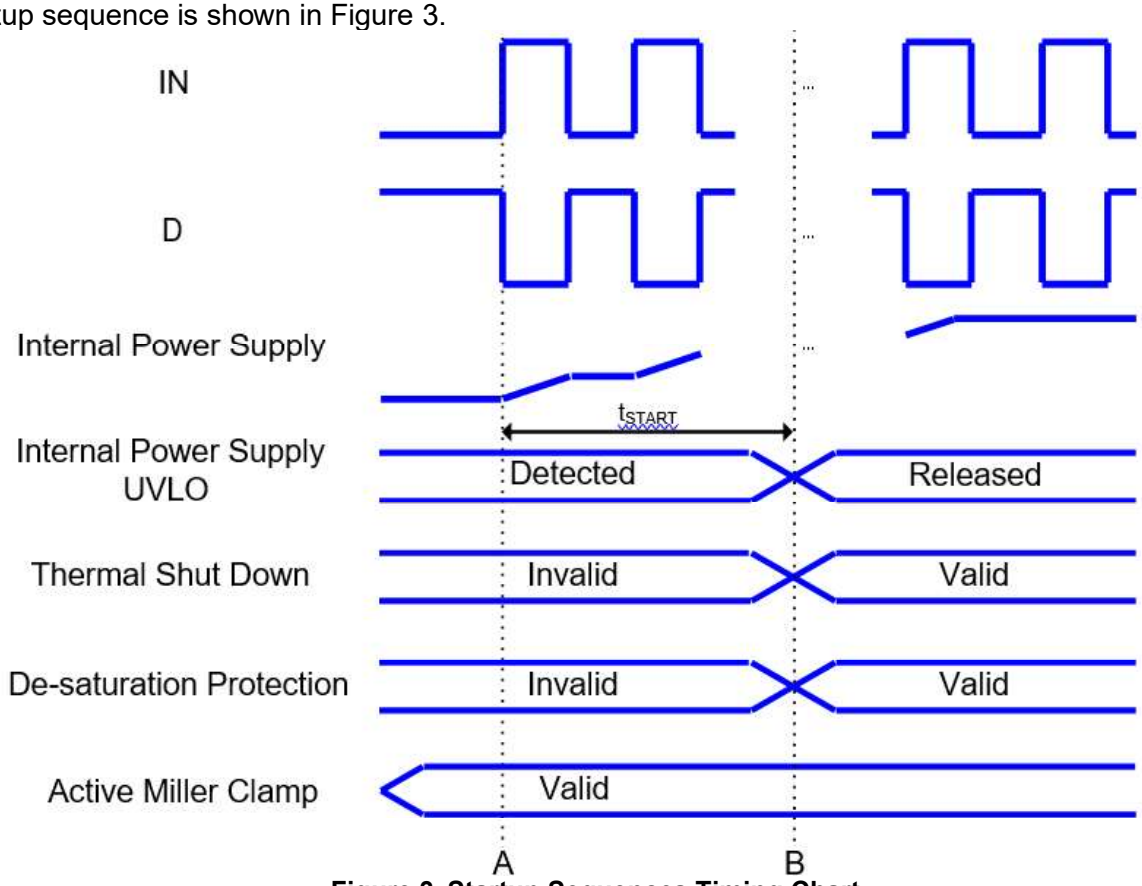


Figure 3. Startup Sequences Timing Chart

A : The IN pin pulse starts to be applied and internal power supply voltage starts to rise. Active miller clamp function is constantly valid.
B : After t_{START} from A, internal power supply UVLO is released and thermal shut down and de-saturation protection function becomes valid.

5. Shut Down Sequence

Shut down sequence is shown in Figure 4.

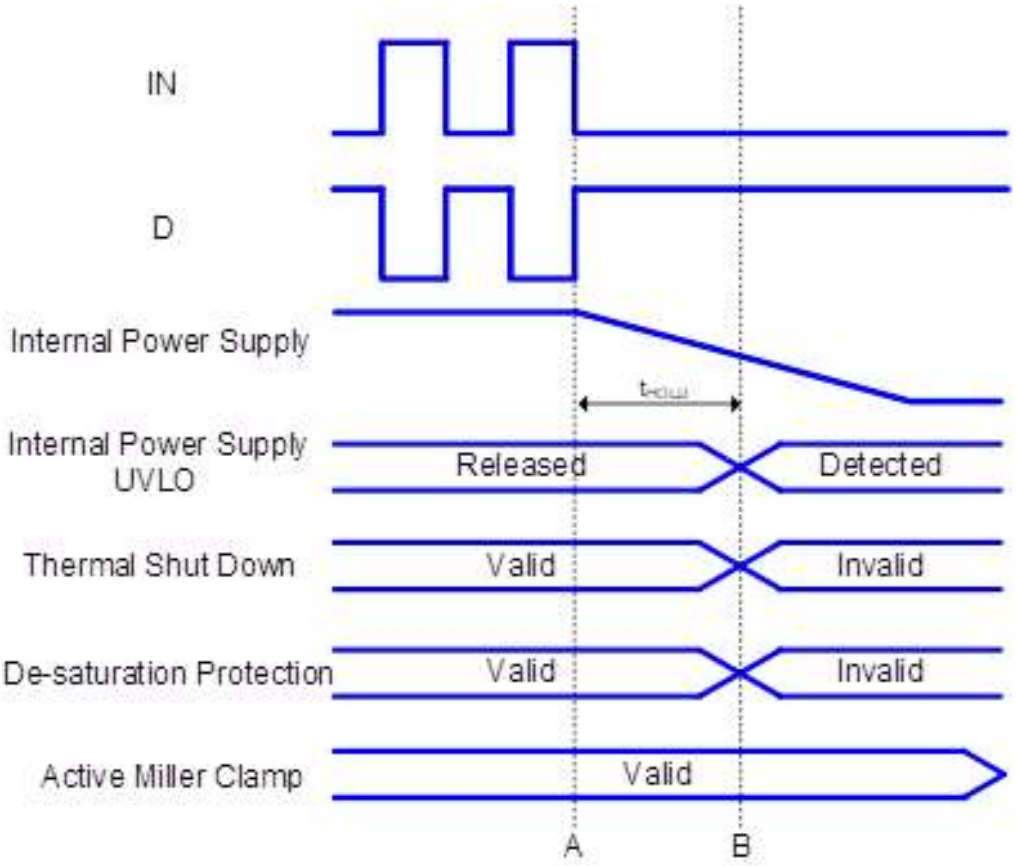


Figure 4. Shut Down Sequence Timing Chart

A : The IN pin pulse stops and internal power supply voltage starts to fall.
B : After t_{HOLD} from A, internal power supply UVLO is detected and thermal shut down and de-saturation protection function becomes invalid. Active miller clamp function is constantly valid.

6. Maximum ratings (Unless noted otherwise, Tj = 25 °C)

Parameter	Symbol	Rating	Unit	Note/Test Condition
Maximum Applied Voltage 1	V_{MAX1A}	-7 to +700	V	D pin voltage, DC
	V_{MAX1B}	-7 to +800	V	D pin voltage, tpulse < 1 µs (Note 1)
Maximum Applied Voltage 2	V_{MAX2A}	-0.3 to +20	V	IN pin voltage, DC
	V_{MAX2B}	-0.3 to +21	V	ININ pin voltage, tpulse < 1 µs (Note 1)
DRAIN Pin Current	$I_{D1(RMS)}$	52.8	A	RMS, Tc = 25 °C
	$I_{D2(RMS)}$	33.4	A	RMS, Tc = 100 °C
	$I_{D3(RMS)}$	23.6	A	RMS, Tc = 125 °C
	$I_{D1(PULSE)}$	72.8	A	tpulse = 1 µs,Duty = 10% Tc = 25 °C
	$I_{D2(PULSE)}$	46.0	A	tpulse = 1 µs,Duty = 10% Tc = 100 °C
	$I_{D3(PULSE)}$	32.5	A	tpulse = 1 µs,Duty = 10% Tc = 125 °C
DRAIN dv/dt	dv/dt	100	V/ns	VD = 0 V to 400 V
Maximum Junction Temperature	Tjmax	150	°C	
Storage Temperature Range	Tstg	-55 to +150	°C	

Caution 1: *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*

Caution 2: *Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.*

(Note 1) Duty is less than 1 %

7. Thermal Resistance *(Note1)*

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Junction to Ambient *(Note2)*	R_{thJA}	-	-	42.8	°C/W	
Junction to Case (Bottom)	$R_{thJC(BOT)}$	-	0.41	0.54	°C/W	

(Note 1) Based on JESD51-2A (Still-Air), JESD51-14.
(Note 2) Using a PCB board based on JESD51-5, 7.

8. Recommended Operating Conditions

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Input Voltage Range 1	V_{IN_H}	8.5	-	20	V	IN pin high voltage
Input Voltage Range 2	V_{IN_L}	-0.3	0	+0.3	V	IN pin low voltage
Turn-on IN Pin Series Resistor	R_{INon}	5	-	220	Ω	
Turn-off IN Pin Series Resistor	R_{INoff}	1		10	Ω	
IN Pin High Pulse-width	t_{IN_H}	75	-	-	ns	
IN Pin Low Pulse-width	t_{IN_L}	75	-	-	ns	
IN Pulse Frequency	f_{IN}	-	-	2	MHz	
Operating Temperature	Topr	-40	-	+125	°C	Surrounding temperature

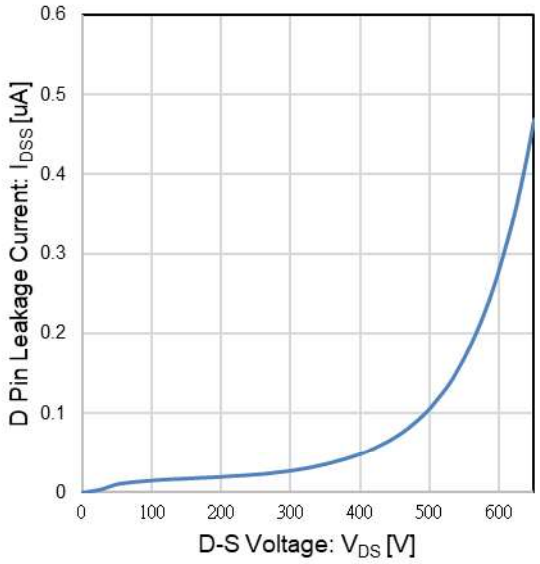
9. Electrical Characteristics (Unless noted otherwise, V_{IN} = 15 V, Tj = 25 °C)

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
GaN HEMT						
D-S Withstand Voltage	$V_{(BR)DSS1}$	-	-	700	V	V_{IN} = 0 V
	$V_{(BR)DSS2}$	-	-	800	V	V_{IN} = 0 V, tpulse < 1 μs *(Note 1)*
D Pin Leak Current	I_{DSS1}	-	0.5	50	μA	V_D = 650 V, V_{IN} = 0 V, Tj = 25 °C
	I_{DSS2}	-	16	-	μA	V_D = 650 V, V_{IN} = 0 V, Tj = 150 °C
D-S ON State Resistance	R_{ON1}	-	40	56	mΩ	I_D = 12.0 A, Tj = 25 °C
	R_{ON2}	-	84	-	mΩ	I_D = 12.0 A, Tj = 150 °C
S-D Reverse Voltage	V_{SD}	-	2.6	-	V	I_D = -12.0 A, V_{IN} = 0 V
Output Capacitance	C_{OSS}	-	74.5	-	pF	V_{IN} = 0 V, V_D = 400 V, f = 1 MHz
Energy Related Effective Output Capacitance	$C_{O(ER)}$	-	108	-	pF	V_{IN} = 0 V, V_D = 0 V to 400 V
Time Related Effective Output Capacitance	$C_{O(TR)}$	-	157	-	pF	V_{IN} = 0 V, V_D = 0 V to 400 V
Output charge	Q_{OSS}	-	62.6	-	nC	V_{IN} = 0 V, V_D = 0 V to 400 V
Reverse Recovery Charge	Q_{RR}	-	0	-	nC	
IN Pin						
IN Operating Current	I_{OPE}	-	10	17	mA	D pin = open, operating at 500 kHz, duty = 50 %
IN Quiescent Current	I_{QUI}	-	1.8	4.1	mA	VIN = 15 V
Switching Characteristics						
Turn-on Delay Time	$t_{D(ON)}$	20	30	40	ns	R_{INON} = 5 Ω, R_{INOFF} = 1Ω I_D = 12A *(Note2)*
Turn-off Delay Time	$t_{D(OFF)}$	4.5	6.5	8.5	ns	R_{INON} = 5 Ω, R_{INOFF} = 1Ω I_D = 12A *(Note2)*
Turn-on Slew Rate	SR_{ON}	-	57.5	-	V/ns	R_{INON} = 5 Ω, R_{INOFF} = 1Ω I_D = 12A *(Note2)*
Turn-off Slew Rate	SR_{OFF}	-	28.6	-	V/ns	R_{INON} = 5 Ω, R_{INOFF} = 1Ω I_D = 12A *(Note2)*
Turn-ON switching energy	E_{ON}	-	19.0	-	uJ	R_{INON} = 5 Ω, R_{INOFF} = 1Ω I_D = 12A
Turn-OFF switching energy	E_{OFF}	-	1.48	-	uJ	R_{INON} = 5 Ω, R_{INOFF} = 1Ω I_D = 12A
Protections						
De-saturation Protection Voltage	V_{DSAT}	IN-5	IN-3	IN-1	V	D Voltage
De-saturation Protection Leading Edge Blanking Time	t_{LEB}	-	200	-	ns	R_{INON} = 5Ω, R_{INOFF} = 1Ω *(Note3)*
De-saturation Protection Propagation Delay	t_{DESAT}	-	80	-	ns	*(Note3)*
TSD Temperature	T_{SD}	150	175	200	℃	
TSD Detection Delay	t_{TSD}	5	10	20	us	
Active Miller Clamp dv/dt	dv/dt_{AMC}	-	-	10	V/ns	D pin rising dv/dt *(Note3)*
Startup Items						
Internal Power Supply Validation Time	t_{START}	-	200	400	us	D pin = open, operating at 500 kHz, duty = 50 %
Internal Power Supply Hold Time	t_{HOLD}	50	-	250	us	V_{IN} = 0 V

(Note 1) Duty is less than 1 %
(Note 2) Refer to "Switching Parameter Measurement information"
(Note 3) Ensured by design, no shipping inspection.

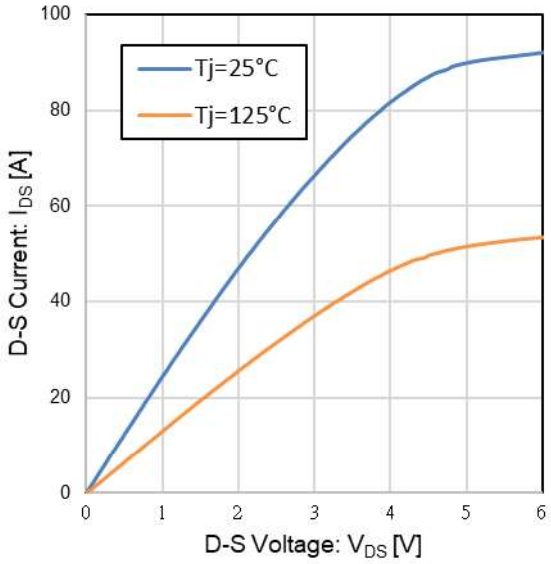
10. Electrical characteristics diagrams

Fig 5. Typ. Drain-source Leakage Current



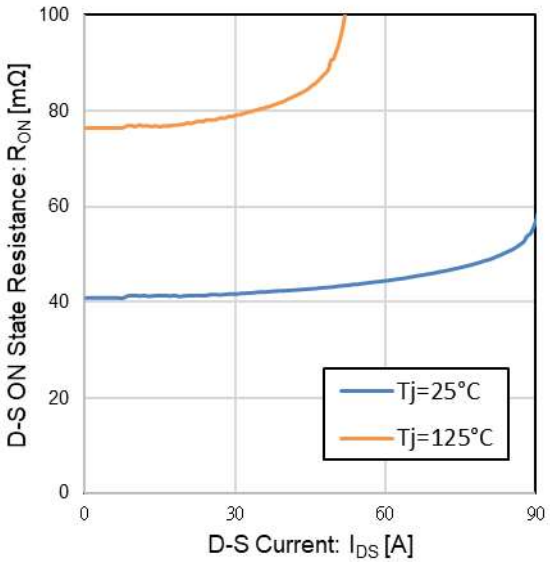
$I_{DSS}=f(V_{DS})$; $T_j=25°C$

Fig 6. Typ. Output characteristics



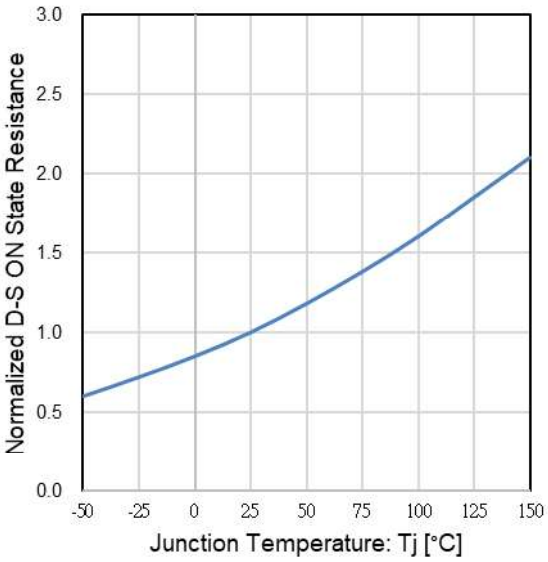
$I_D=f(V_{DS})$; $T_j=25°C$, 125°C

Fig 7. Typ. Drain-source on-state resistance



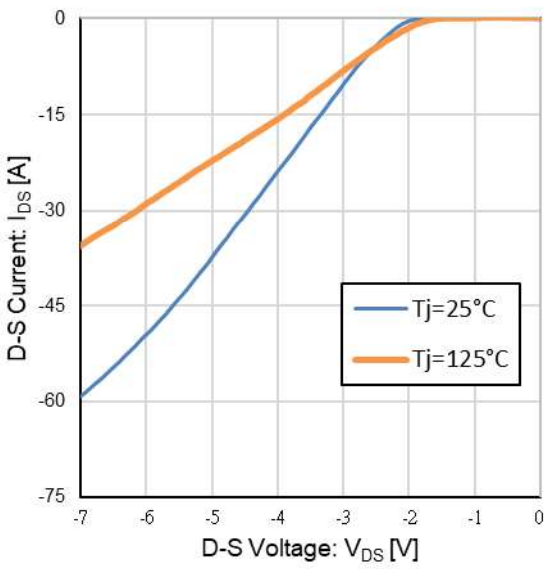
$R_{DS(on)}=f(I_D)$; $T_j=25°C$, 125°C

Fig 8. Typ. Drain-source on-state resistance



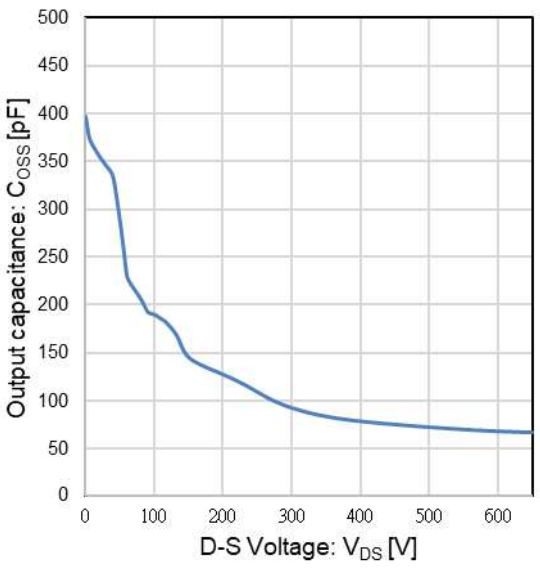
$R_{DS(on)}=f(T_j)$; $I_D=12A$

Fig 9. Typ. channel reverse characteristics



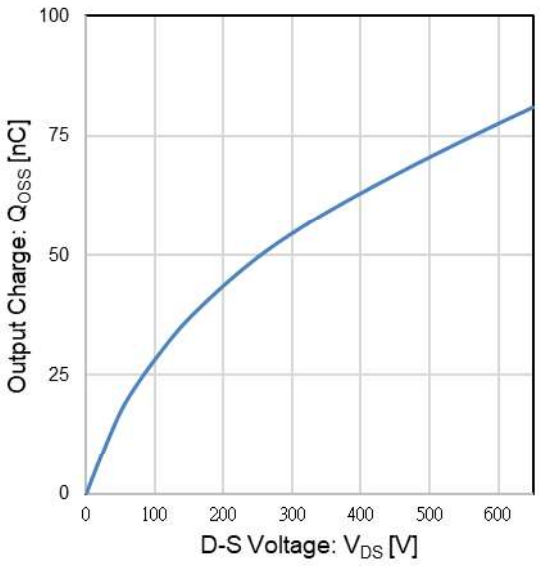
$V_{DS}=f(I_D)$; $T_j=25°C$, 125°C

Fig 10. Typ. Capacitance



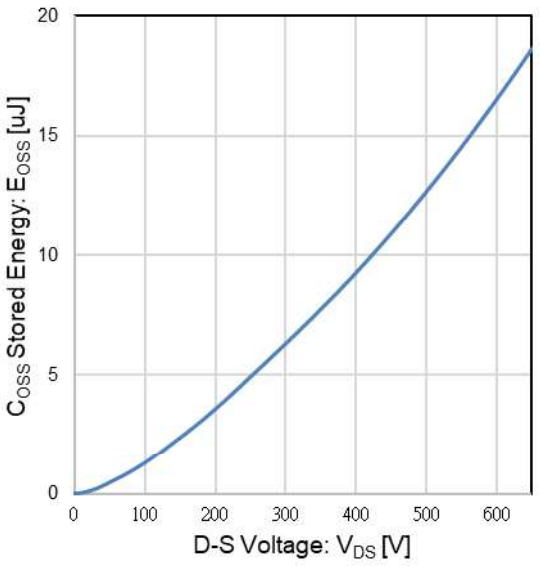
C=f(V_{DS}); V_{DS}=650V; parameter: T_j=25°C

Fig 11. Typ. Qoss



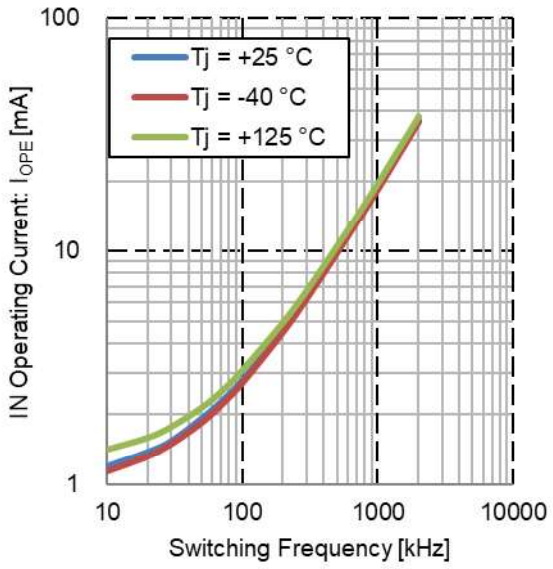
$Q_{oss}=f(V_{DS})$

Fig 12. Typ. Coss stored energy



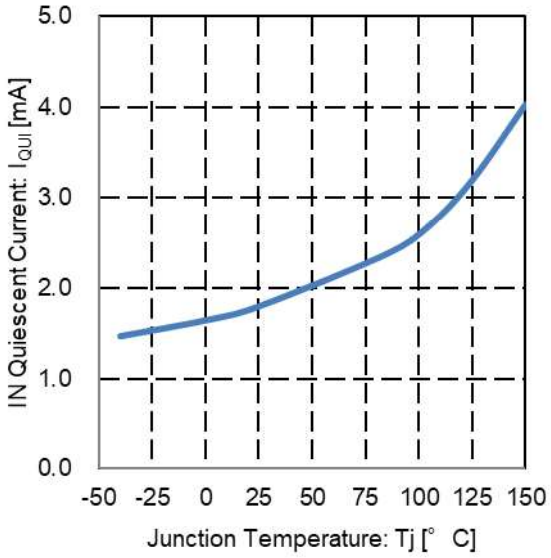
$E_{oss}=f(V_{DS})$

Fig 13. IN Operating Current vs Switching Frequency



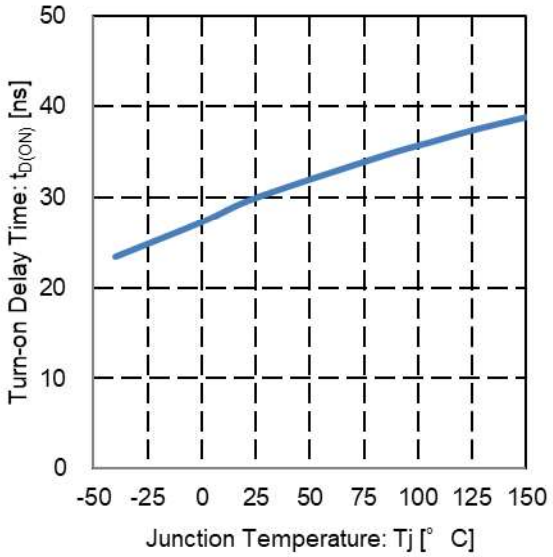
I_{OPE}=f(Freq.); T_j= -40°C, 25°C, 125°C

Fig 14. IN Quiescent Current vs Junction Temperature



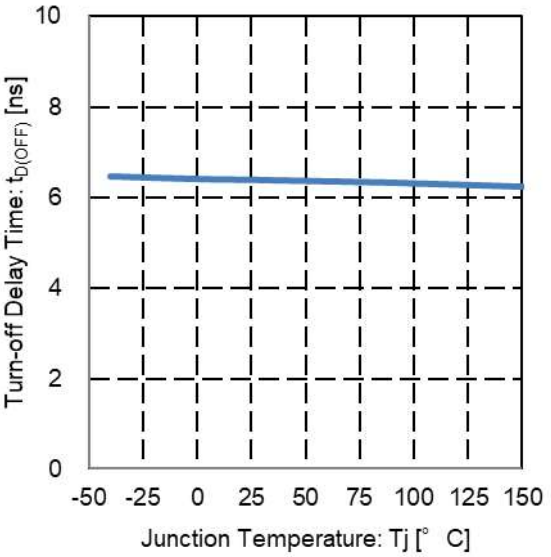
I_{QUI}=f(T_j.)

Fig 15. Turn-on Delay Time vs Junction Temperature



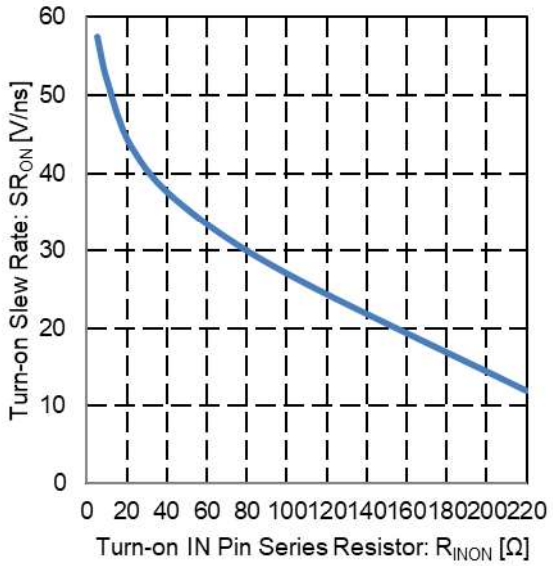
$t_{D(ON)}$=f(T_j.)

Fig 16. Turn-off Delay Time vs Junction Temperature



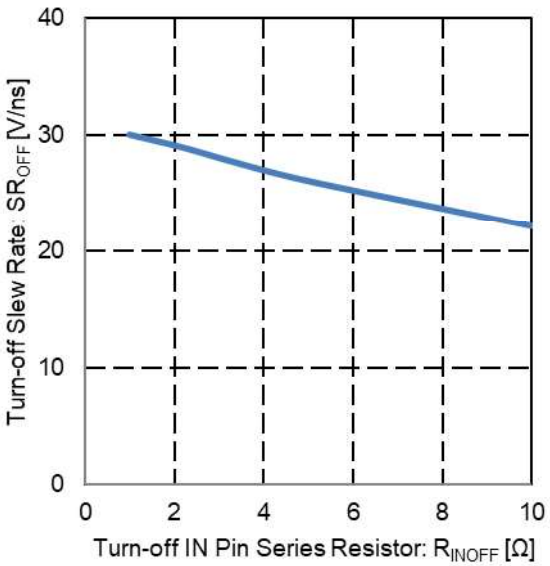
$t_{D(OFF)}$=f(T_j.)

Fig 17. Turn-on Slew Rate vs Turn-on IN Pin Series Resistor



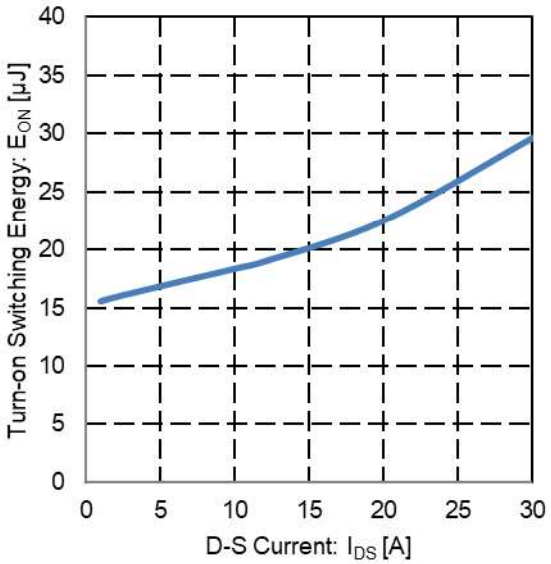
$SR_{ON}=f(R_{INON})$

Fig 18. Turn-off Slew Rate vs Turn-off IN Pin Series Resistor



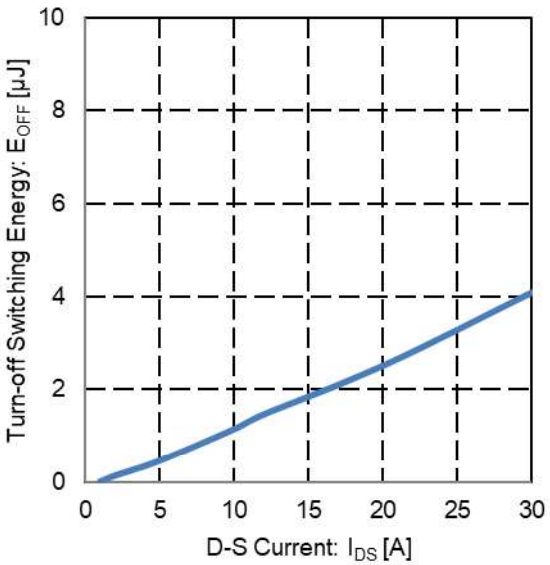
$SR_{OFF}=f(R_{INOFF})$

Fig 19. Turn-on Switching Energy vs D-S Current



$E_{ON}=f(I_{DS})$

Fig 20. Turn-off Switching Energy vs D-S Current



$E_{OFF}=f(I_{DS})$

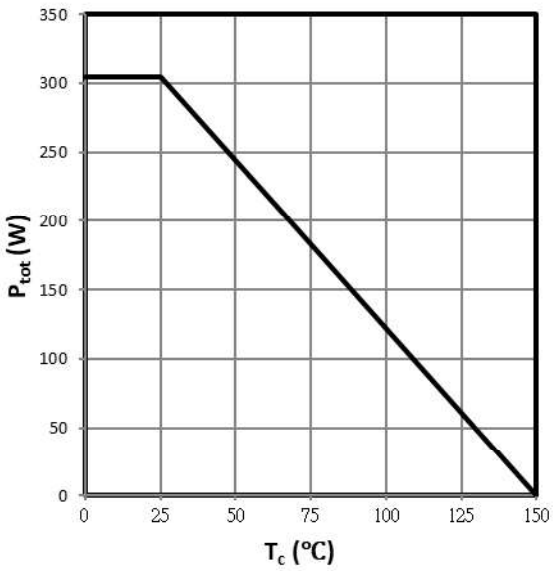
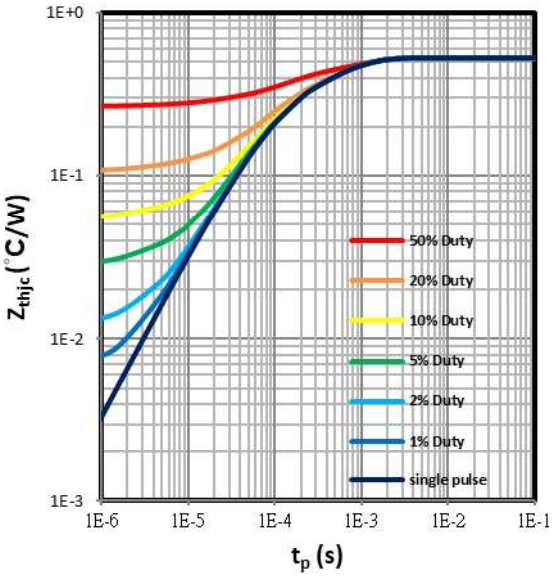
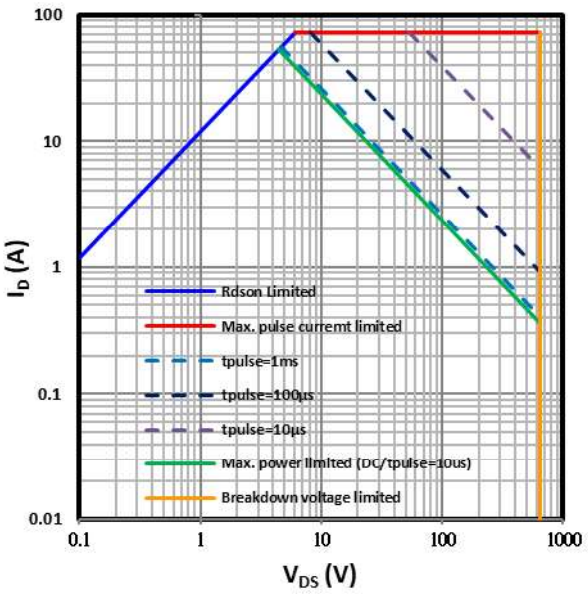
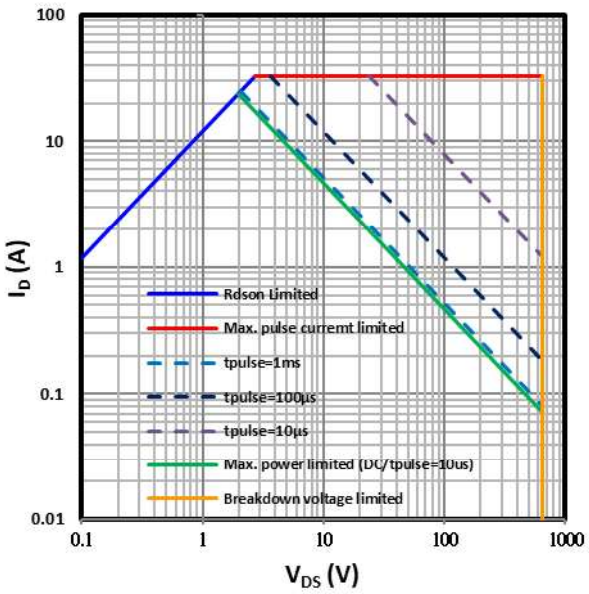
Fig 21. Power Dissipation	Fig 22. Max. transient thermal impedance
	
$P_{tot}=f(T_c)$	$Z_{thjc}=f(t_p, D)$

Fig 23. Safe operating area T_c=25°C	Fig 24. Safe operating area T_c=125°C
	
$I_D=f(V_{DS})$; Duty=50%; parameter: t_P	$I_D=f(V_{DS})$; Duty=50%; parameter: t_P

11. Switching Parameter Measurement Information

Figure 25 shows the circuit for measurements of switching parameters.
Figure 26 shows instruction of them.

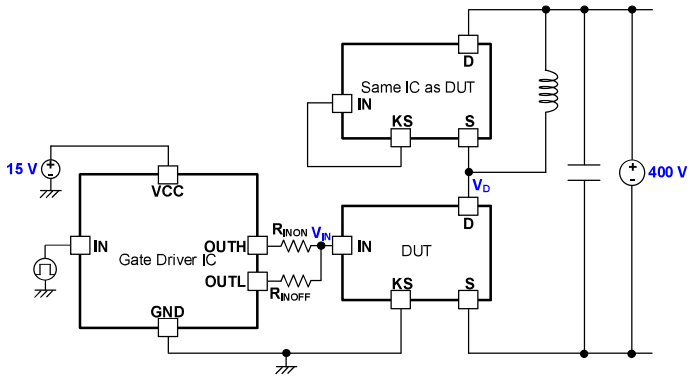


Figure 25. Switching Parameters Measurement Circuit

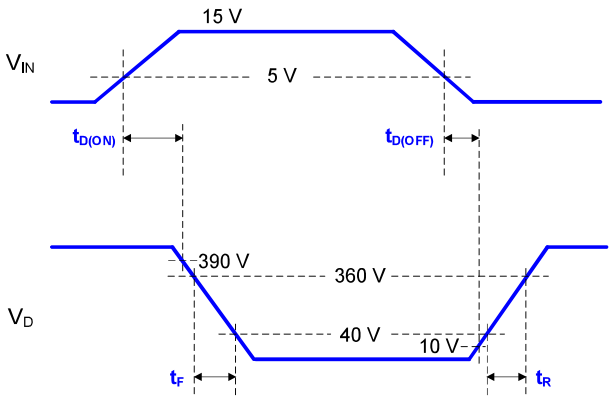


Figure 26. Instruction of Switching Parameters

11.1 Turn-on Delay Time: $t_{D(ON)}$

The turn-on delay time is the time from rising edge of the IN pin voltage (represented by V_{IN} rising to 5 V) to when the GaN HEMT starts turning on (represented by V_D falling to 390 V).

11.2 Drain Fall Time: t_F

The drain fall time is the time it takes for V_D falls from 360 V to 40 V.

11.3 Turn-off Delay Time: $t_{D(OFF)}$

The turn-off delay time is the time from falling edge of the IN pin voltage (represented by VIN falling to 5 V) to when the GaN HEMT starts turning off (represented by VD rising to 10 V).

11.4 Drain Rise Time: t_R

The drain rise time is the time it takes for VD rises from 40 V to 360 V.

11.5 Turn-on Slew Rate: SR_{ON}

The turn-on slew rate is the slew rate which is when VD falls from 360V to 40V of VBUS.
It is calculated by the formula below.

$$SR_{on} = \frac{320V}{t_F}$$

where:
SR_{ON} is the turn-on slew rate.
t_F is the drain fall time.

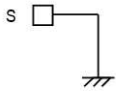
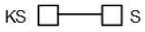
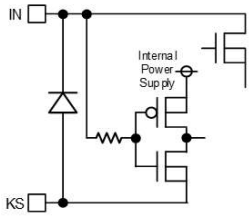
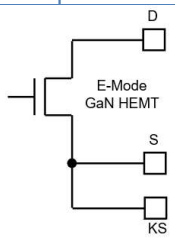
11.6 Turn-off Slew Rate: SR_{OFF}

The turn-off slew rate is the slew rate which is when VD rises from 40V to 360V of VBUS.
It is calculated by the formula below.

$$SR_{off} = \frac{320V}{t_R}$$

where:
SR_{OFF} is the turn-off slew rate.
t_R is the drain rise time.

12. I/O Equivalence Circuit

5-6, 9	S	7	KS	8	IN	1-4	D
							

13. Operational Notes

13.1 Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

13.2 Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

13.3 Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

13.4 Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

13.5 Recommended Operating Conditions

The function and operation of the IC are guaranteed within the range specified by there commended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

13.6 Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

13.7 Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

13.8 Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

13.9 Unused Input Pins

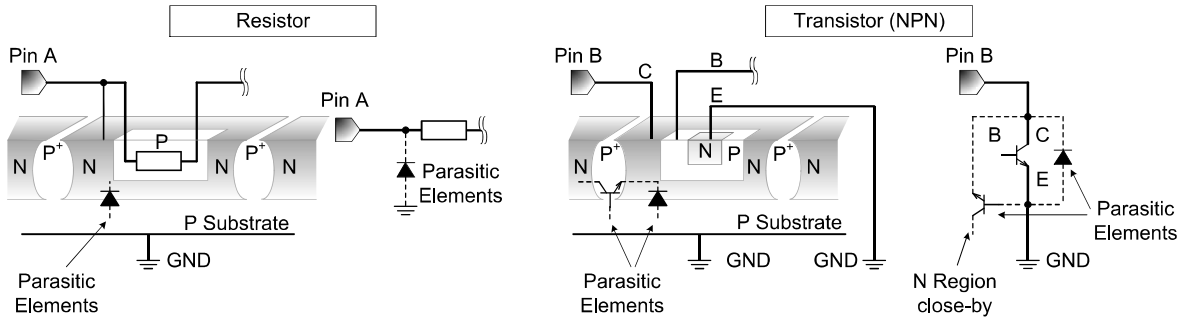
Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

13.10 Regarding the Input Pin of the IC

This IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.



13.11 Ceramic Capacitor

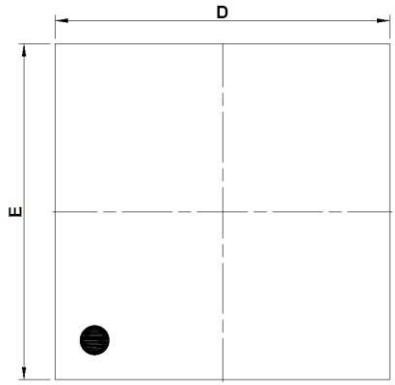
When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

13.12 Thermal Shutdown Circuit(TSD)

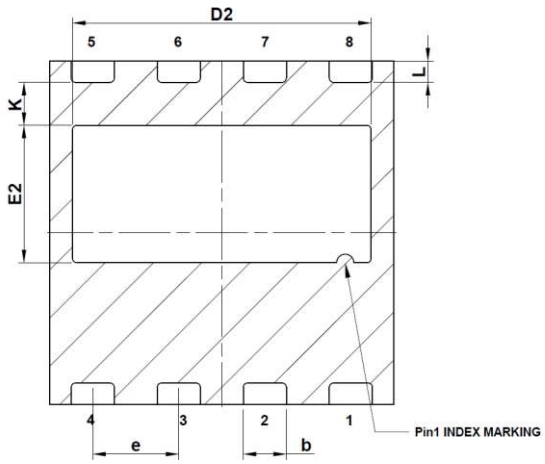
This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF power output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

Table 1. Package outlines

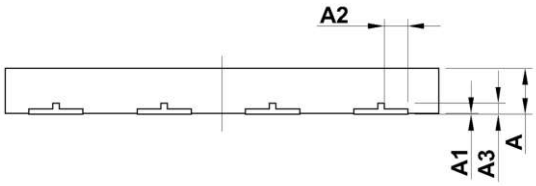
Top View

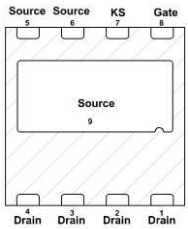


Bottom View



Side view

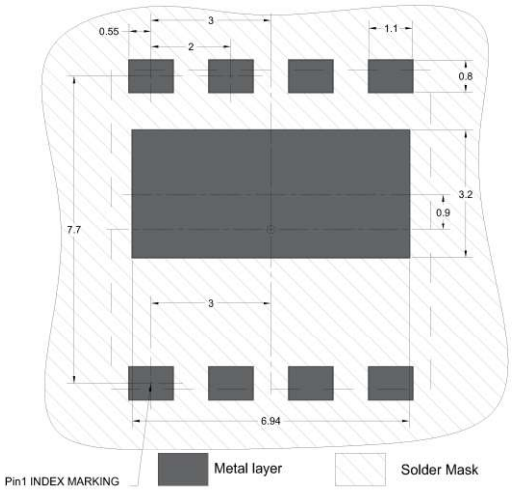




SYMBOLS	DIMENSIONS IN MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.75	0.85	0.95
A1	0.00	0.02	0.05
A2		0.44 REF	
A3		0.203 REF	
b	0.95	1.00	1.05
D	7.90	8.00	8.10
D2	6.84	6.94	7.04
E	7.90	8.00	8.10
E2	3.10	3.20	3.30
e		2.00 REF	
K		1.00 REF	
L	0.45	0.50	0.55

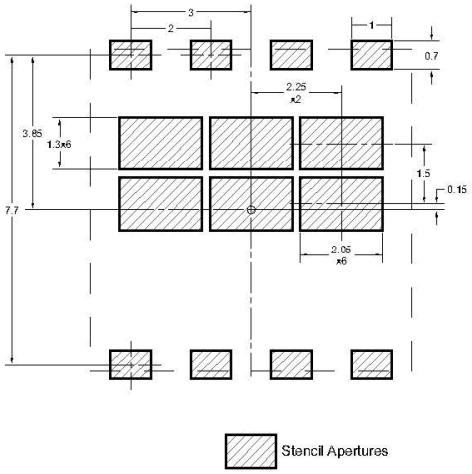
Table 2. **Recommended PCB Footprint & Stencil**

Recommended PCB Footprint



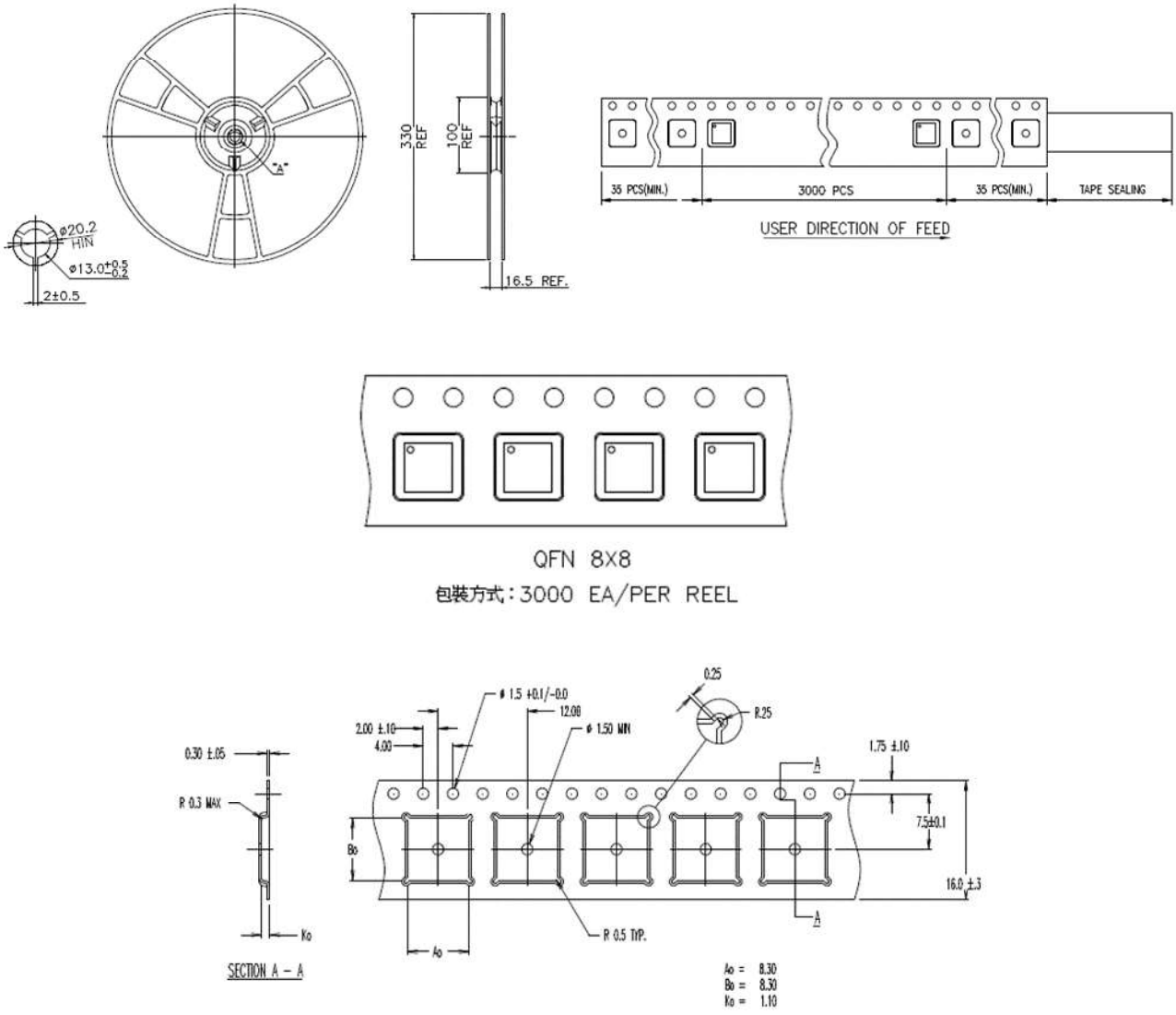
All dimensions are in units mm.
All pads are solder mask define.

Recommended Stencil apertures



Thickness of steel plate: 100um

Table 3. Tape and reel configuration.



All dimensions are in units mm.